REMARKS

Claims 1 through 26 are in the application, with no claim amendments having been made in this paper. No new matter has been added. Claims 1, 9, 15 and 19 are the independent claims herein. Reconsideration and further examination are respectfully requested.

(The title of the application has now been amended in accordance with the Examiner's suggestion.)

Claim Rejections – 35 USC § 102

Claims 1-2, 5-10, 13-20, and 23-26 are rejected under 35 U.S.C. 102 as being anticipated by Krone et al. U.S. Patent No. 7,003,023.

Claim 1 is directed to an "apparatus" that includes "a line side circuit" and "a system side circuit to couple to the line side circuit via an isolation interface". Claim 1 further recites that the system side circuit includes "a first clock signal generator to supply a first clock signal to the line side circuit via the isolation interface" and "a second clock signal generator to supply a second clock signal to the line side circuit via the isolation interface". In addition, claim 1 specifies that "the first and second clock signals when added sum to a signal having a substantially constant voltage".

Applicants respectfully traverse the rejection of claim 1. Applicants submit that the Examiner has failed to carefully read the claim language on Krone's circuitry, and therefore has erred in rejecting claim 1.

Applicants concede that there are similarities between Krone's circuitry and the circuit recited in claim 1, and applicants further concede that Krone's circuitry provides some similar benefits to that provided by the claimed circuitry. Nevertheless, there are also significant differences--that the Examiner apparently has not appreciated--between the claims herein and the circuitry shown in the reference.

To note a first discrepancy in the rejection of claim 1 (as set forth in the pending Office Action), the Examiner refers--at page 2, last paragraph of the Office Action--to "first and second clock drivers", which the Examiner considers satisfied by element 214 in FIG. 2 of the Krone reference. However, applicants respectfully point out that the language of claim 1 recites first and second "clock signal generators", not "clock drivers".

More fundamentally, the signals driven across the isolation barrier (209 and 210 in FIG. 2 of Krone) constitute a differential data signal, not clock signals. In this regard, the Examiner is respectfully referred to column 8, lines 9-11 in Krone. ("The clock recovery circuit recovers a clock signal from the digital data driven across the isolation barrier." [emphasis added]) The passage at column 7, line 60 to column 8, line 2 of Krone is to the same effect:

> In one embodiment of the present invention, driver circuit 214 drives the transmit side of capacitor 209 with a digital voltage signal. Clock recovery circuit 216 presents a very high impedance to the receive side of capacitor 209, allowing the digital voltage output of driver 214 to couple across the isolation barrier. In this embodiment, capacitor 210 provides a return current path across the barrier. In another embodiment, capacitors 209, 210 are differentially driven by complementary digital outputs of driver circuit 214. [emphasis added]

In other words, in one embodiment of Krone's circuit, a data signal is transmitted across one capacitor and the other capacitor provides a return path--clearly in this embodiment it is not the case that two clock signals are transmitted across the capacitors. In the other embodiment, a differential data signal (again, not clock signals) is transmitted across the capacitors.

This reading of the Krone reference is further reinforced by the point that if the signals transmitted across the capacitors 209, 210 were clock signals, as the Examiner apparently contends, then there would be no need to recover (cf. clock recovery circuit 216 in FIG. 2 of Krone) a clock signal from the signal transmitted across the capacitors. Still further, if the signals across 209 and 210 were clock signals, there would be nothing to decode (cf. decoder 217 in FIG. 2 of Krone).

To summarize, the circuitry shown in FIG. 2 of the Krone reference simply lacks the claimed first and second clock signal generators which supply first and second clock signals to the line side circuit via the isolation barrier. The signal driven across capacitors 209 and 210 by driver 214 in Krone's circuitry is a data signal, not a differential clock signal. It follows that the pending rejection of claim 1 should be reconsidered and withdrawn.

The above remarks regarding claim 1 are equally applicable to two of the three other independent claims, namely to claims 9 and 19. Accordingly claims 9 and 19 are submitted as

patentable over Krone on the same basis as claim 1. As to claim 15 (which is the only other independent claim), a brief further explanation is in order.

Claim 15 is directed to a "method", which includes "supplying a first clock signal from a system side circuit to a line side circuit via an isolation interface" and "supplying a second clock signal from the system side circuit to the line side circuit via the isolation interface". In addition, claim 15 specifies that "the first and second clock signals when added sum to a signal having a substantially constant voltage".

Briefly recapping the above discussion of the Krone reference, the circuit in Krone transmits a data signal across an isolation barrier, but does not transmit a clock signal (much less two clock signals) across the isolation barrier. For this reason, claim 15, like the other independent claims, is patentably distinguished from the Krone reference.

Applicants respectfully request that the Examiner recognize the significant differences between the claimed invention and the Krone reference by withdrawing the pending rejections.

CONCLUSION

Accordingly, Applicants respectfully request allowance of the pending claims. If any issues remain, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is kindly invited to contact the undersigned via telephone at (203) 972-3460.

Respectfully submitted,

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